LC2333B

16V 3A Synchronous PFM/PWM Buck Converter

DESCRIPTION

The LC2333B is a high efficiency current-mode synchronous, 16V/3A buck converter. Its input voltage ranges from 4.2V to 16V and it provides an adjustable regulated output voltage from 1V to 12V while delivering up to 3A of output current.

The internal synchronous switches increase efficiency and eliminate the need for an external Schottky diode. The switching frequency is set to 500KHz. And the LC2333B will automatically switch between PFM and PWM mode based on the load current, thus to enhance the converter efficiency at light load.

The LC2333B is available in the ESOP-8 package.

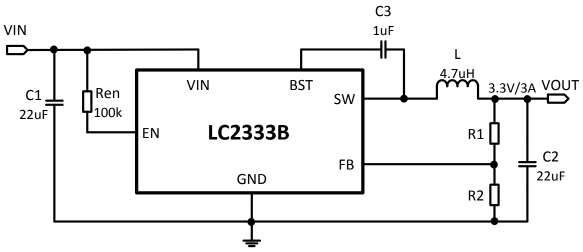
FEATURES

- High Efficiency: Up to 96%
- 500KHz Frequency Operation
- 3A Output Current
- No Schottky Diode Required
- 4.2V to 16V Input Voltage Range
- 0.923V Reference
- Slope Compensated Current Mode Control for Excellent Line and Load Transient Response
- Integrated internal compensation
- Stable with Low ESR Ceramic Output Capacitors
- Over Current Protection with Hiccup-Mode
- Thermal Shutdown
- Inrush Current Limit and Soft Start
- Available in ESOP-8
- -40°C to +85°C Temperature Range

APPLICATIONS

- Set-top-box
- Consumer Electronic Device for automobile
- LCD Monitor and LCD TV
- Portable DVD
- ADSL Modem, WLAN router
- Other 12V or double cell Li-ion battery powered device

TYPICAL APPLICATION



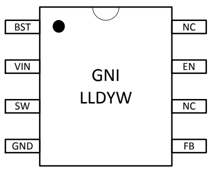
Note:1) $V_{OUT} = \left(1 + \frac{R_1}{R_2}\right) \times V_{FB}$

2) C1 and C2 recommended using 22uF ceramic capacitors. If the electrolytic capacitor is used, it is recommended that the ceramic capacitor in parallel with a capacitance value of 0.1uF or more.

3) The value of R1 is recommended to be about 300kΩ.

4) C3 can be valued as 1uF, 0.1uF.

PIN OUT



ESOP-8

ORDERING INFORMATION

Mark Explanation	*Ordering Information*	
GN: Product Code LL: Lot No. D: Fab code *YW: Date code*	ESOP-8 2500pcs/reel	LC2333BCS8TR

PINOUT DESCRIPTION

PIN #	NAME	DESCRIPTION
1	BST	High side power transistor gate drive boost input.
2	VIN	Power input. Bypass with a 10uF~22uF ceramic capacitor to GND.
3	SW	Power switching node to connect inductor.
4	GND	Ground.
5	FB	Feedback input with reference voltage set to 0.923V.
6	NC	No connection
7	EN	Enable input. Set this pin to high level to enable the part, low level to disable.
8	NC	No connection

ABSOLUTE MAXIMUM RATING

Parameter		Value
Max Input Voltage		20V
Max Operating Junction Temperature(Tj)		150°C
Ambient Temperature(Ta)		-40°C – 85°C
Package Thermal Resistance (θjc)	ESOP-8	10°C / W
Storage Temperature(Ts)		-40°C - 150°C
Lead Temperature & Time		260°C, 10S

***Note**: Exceed these limits to damage to the device. Exposure to absolute maximum rating conditions may affect device reliability.*

RECOMMENDED WORK CONDITIONS

Parameter	Value
Input Voltage Range	Max. 16V
Operating Junction Temperature(Tj)	-40°C –125°C

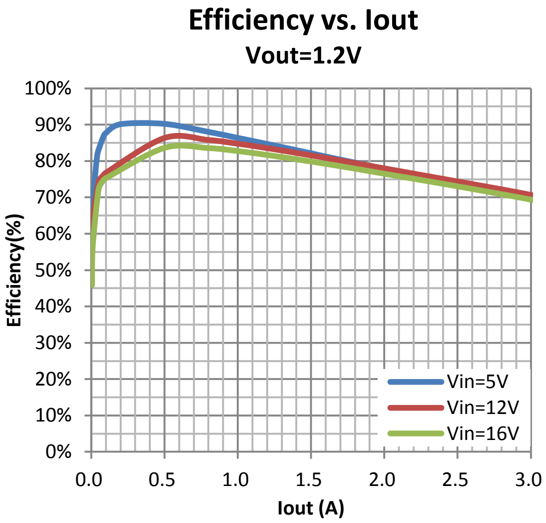
ELECTRICAL CHARACTERISTICS

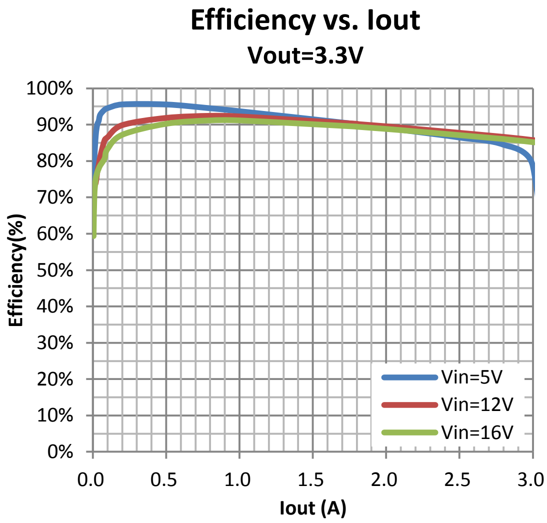
(VIN=12V, T_A=25°C)

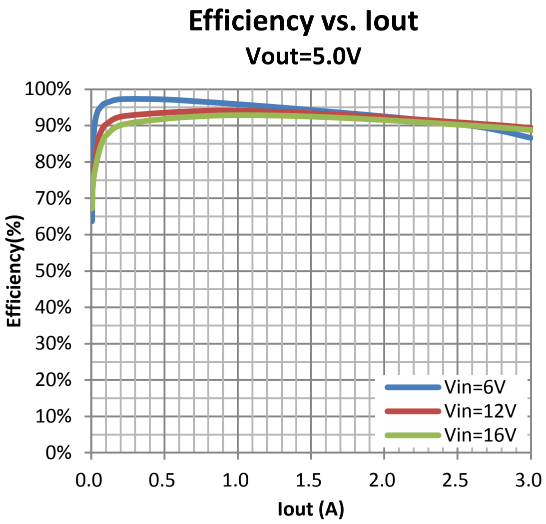
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VDD	Input Voltage Range		4.2		16	V
Vref	Feedback Voltage	Vin=12V, Ven=5V	0.905	0.923	0.941	V
V_{UVLO}	UVLO Voltage	Vin H-->L, Iout=0.5A		4.1		V
Iq	Quiescent Current	Active, Vfb=1V, No Switching		0.5		mA
		Shutdown, Vin=8V		5	10	uA
Fsoc	Switching Frequency	Ven=2V, Vin=12V		500		KHz
RdsonN	NMOS Rdson			130		mohm
RdsonN	NMOS Rdson			70		mohm
Ilimit	Peak Current Limit			3.8		A
Venh	EN High Threshold		1.5			V
Venl	EN Low Threshold				0.6	V
D_{MAX}	Maximum Duty Cycle	V_{FB} = 0.7V		92		%
	Minimum On Time			100		ns
TSD	Over Temperature Proection			160		°C
	Thermal Shutdown Hystersis			20		°C

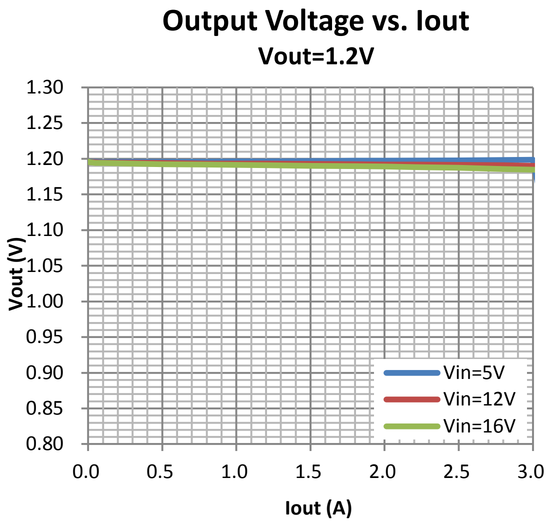
TYPICAL PERFORMANCE CHARACTERISTICS

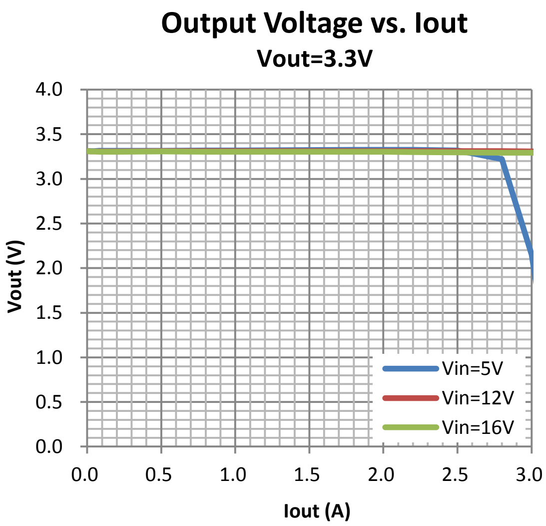
(L=4.7uH, Cin=22uF, Cout=22uF, T_A=25°C, unless otherwise stated)

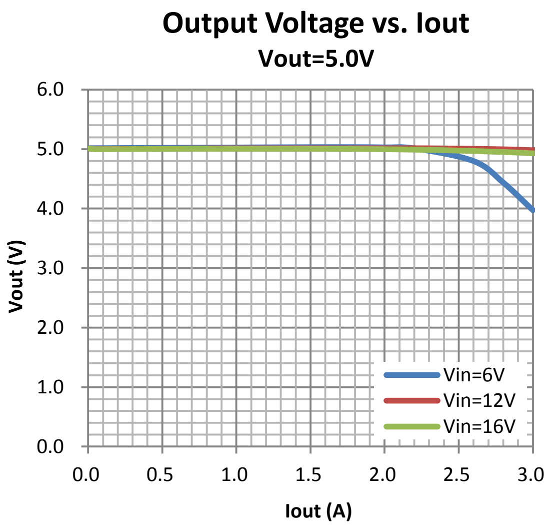






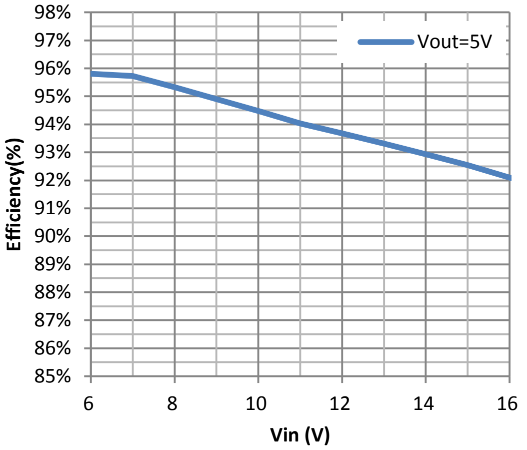






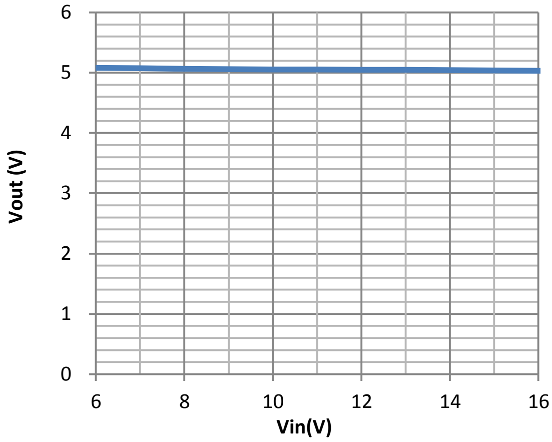
Efficiency vs. Vin

Iout=1A



Vout vs. Vin

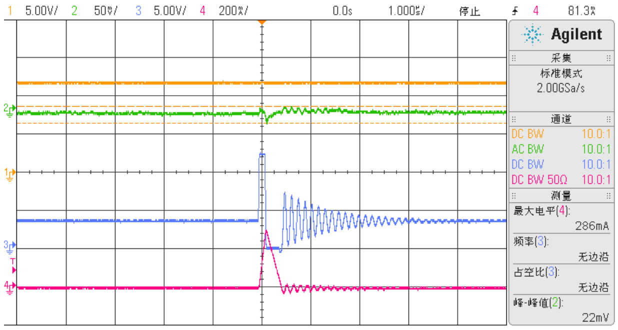
Iout=1A



Switching waveform

Vin=12V, Vout=3.3V, Iout=5mA

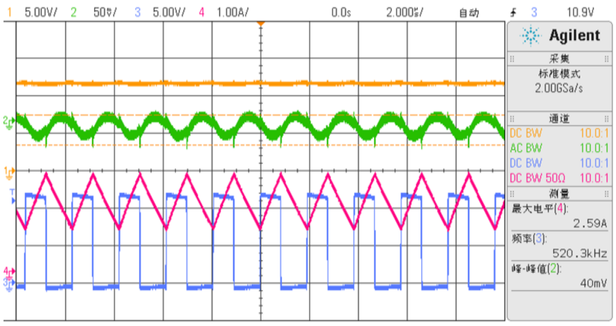
(CH1=Vin, CH2=Vout, CH3=SW, CH4=Isw)



Switching waveform

Vin=12V, Vout=3.3V, Iout=2A

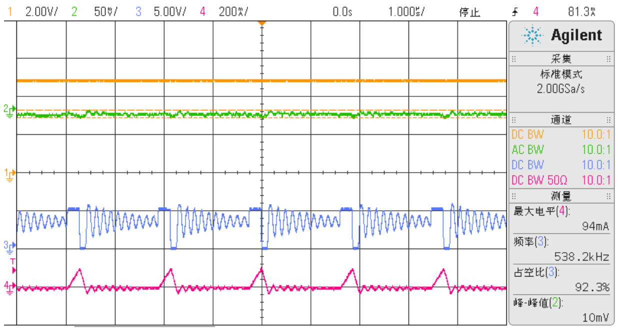
(CH1=Vin, CH2=Vout, CH3=SW, CH4=Isw)



Switching waveform

Vin=5V, Vout=3.3V, Iout=5mA

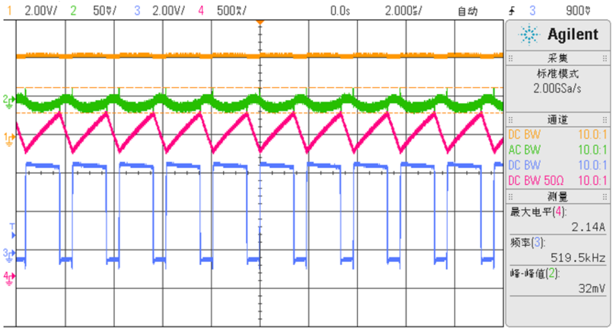
(CH1=Vin, CH2=Vout, CH3=SW, CH4=Isw)



Switching waveform

Vin=5V, Vout=3.3V, Iout=2A

(CH1=Vin, CH2=Vout, CH3=SW, CH4=Isw)



FUNCTIONAL DECRIPTIONS

Internal Regulator

The LC2333B is a current mode step down DC/DC converter that provides excellent transient response with no extra external compensation components. This device contains an internal, low resistance, high voltage power MOSFET, and operates at a high 500K operating frequency to ensure a compact, high efficiency design with excellent AC and DC performance.

Error Amplifier

The error amplifier compares the FB pin voltage with the internal FB reference (V_{FB}) and outputs a current proportional to the difference between the two. This output current is then used to charge or discharge the internal compensation network to form the COMP voltage, which is used to control the power MOSFET current. The optimized internal compensation network minimizes the external component counts and simplifies the control loop design.

Internal Soft-Start

The soft-start is important for many applications because it eliminates power-up initialization problems. The controlled voltage ramp of the output also reduces peak inrush current during start-up, minimizing start-up transient events to the input power bus.

Over-Current-Protection and Hiccup

The LC2333B has a cycle-by-cycle over-current limit for when the inductor current peak value exceeds the set current-limit threshold. First, when the output voltage drops until FB falls below the Under-Voltage (UV) threshold to trigger a UV event, the LC2333B enters hiccup mode to periodically restart the part. This protection mode is especially useful when the output is dead-shorted to ground. This greatly reduces the average short-circuit current to alleviate thermal issues and to protect the regulator. The LC2333B exits hiccup mode once the overcurrent condition is removed.

Startup and Shutdown

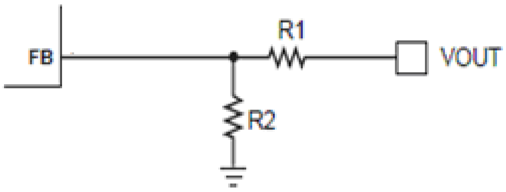
If both VIN and EN are higher than their appropriate thresholds, the chip starts. The reference block starts first, generating stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides stable supply for the remaining circuitries. Three events can shut down the chip: EN low, VIN low and thermal shutdown. In the shutdown procedure, the signaling path is first blocked to avoid any fault triggering. The COMP voltage and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

APPLICATIONS INFORMATION

Setting Output Voltages

The external resistor divider is used to set the output voltage (see Typical Application on page 1). The feedback resistor R1 also sets the feedback loop bandwidth with the internal compensation capacitor. Choose R1 to be around 300kΩ for optimal transient response. R2 is then given by:

$$R_2 = \frac{R_1}{V_{out}/V_{FB} - 1}$$



Selecting the Inductor

Use a 2.2µH-to-10µH inductor with a DC current rating of at least 25% percent higher than the maximum load current for most applications. For highest efficiency, select an inductor with a DC resistance less than 15mΩ. For most designs, derive the inductance value from the following equation.

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{osc}}$$

Where ΔIL is the inductor ripple current. Choose an inductor current approximately 30% of the maximum load current. The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Under light-load conditions (below 100mA), use a larger inductor to improve efficiency.

Selecting the Output Capacitor

The output capacitor (C2) maintains the DC output voltage. Use ceramic, tantalum, or low-

ESR electrolytic capacitors. Use low ESR capacitors to limit the output voltage ripple. Estimate the output voltage ripple with:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L} \times \left[1 - \frac{V_{OUT}}{V_{IN}}\right] \times \left[R_{ESR} + \frac{1}{8 \times f_S \times C_2}\right]$$

Where L is the inductor value and R_{ESR} is the equivalent series resistance (ESR) of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes most of the output voltage ripple. For simplification, estimate the output voltage ripple with:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L \times C_2} \times \left[1 - \frac{V_{OUT}}{V_{IN}}\right]$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with:

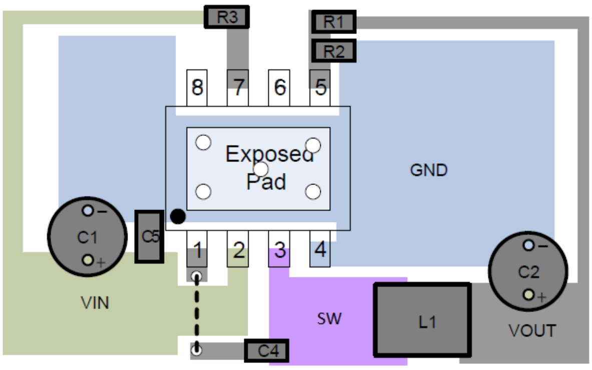
$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L} \times \left[1 - \frac{V_{OUT}}{V_{IN}}\right] \times R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system. The LC2333B can be optimized for a wide range of capacitance and ESR values.

PCB LAYOUT RECOMMENDATION

The device's performance and stability are dramatically affected by PCB layout. It is recommended to follow these general guidelines shown as below:

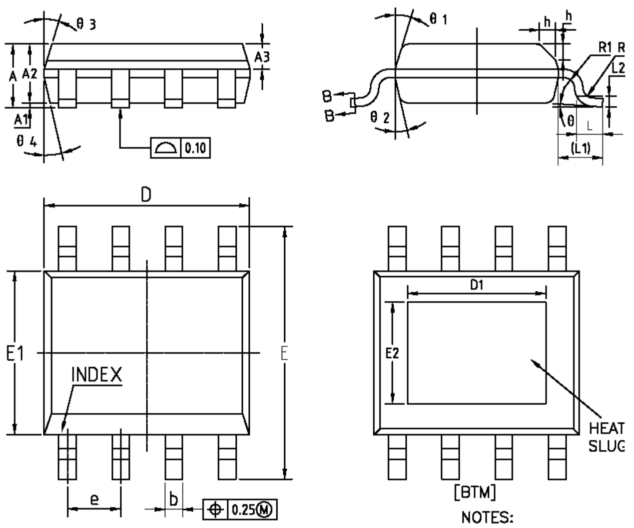
1. Place the input capacitors and output capacitors as close to the device as possible. The traces which connect to these capacitors should be as short and wide as possible to minimize parasitic inductance and resistance.
2. Place feedback resistors close to the FB pin.
3. Keep the sensitive signal (FB) away from the switching signal (SW).
4. The exposed pad of the package should be soldered to an equivalent area of metal on the PCB. This area should connect to the GND plane and have multiple via connections to the back of the PCB as well as connections to intermediate PCB layers. The GND plane area connecting to the exposed pad should be maximized to improve thermal performance.
5. Multi-layer PCB design is recommended.



PACKAGE OUTLINE

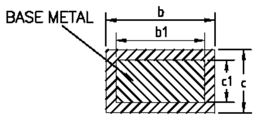
Package	ESOP8	Devices per reel	2500	Unit	mm

Package specification：



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0	0.10	0.15
A2	1.25	1.40	1.65
A3	0.50	0.60	0.70
b	0.38	–	0.51
b1	0.37	0.42	0.47
c	0.17	–	0.25
c1	0.17	0.20	0.23
D	4.80	4.90	5.00
D1	3.10	3.30	3.50
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
E2	2.20	2.40	2.60
e	1.27BSC		
L	0.45	0.60	0.80
L1	1.04REF		
L2	0.25BSC		
R	0.07	–	–
R1	0.07	–	–
h	0.30	0.40	0.50
θ	0°	–	8°
θ 1	15°	17°	19°
θ 2	11°	13°	15°
θ 3	15°	17°	19°
θ 4	11°	13°	15°



SECTION B–B

NOTES:
ALL DIMENSIONS REFER TO JEDEC STANDARD MS–012 AA
DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.